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TURBOchannel
Hardware Specification

On-line version.

Previous versions of this document are obsolete and should be discarded. This document supersedes all previous versions.

Digital Equipment Corporation

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ABOUT THIS SPECIFICATION

Important Changes in the TURBOchannel Hardware Specification. This version of the TURBOchannel Hardware Specification includes all changes made since the original Specification was released. Revision bars mark changes that first appear in this version of the Specification.

The following are the changes that occurred in each version of the Developer's Kit:

Changes in Version 2.0

- *General Description*, paragraph four: Added to indicate that systems can time-multiplex multiple option slots onto a single memory port, or dedicate a memory port to each option slot. Note that systems dedicating a memory port to each slot may have clock frequency, clock phase, and slot address space discontinuities between slots.
- *Signals*, table: Edited to indicate that signal *~err* is used for all forms of DMA error. Systems with parity checking enabled for a slot can assert *~err* if parity errors are detected on the *ad* signals during DMA transactions. The previous description did not list parity errors.
- *I/O Transactions*, paragraph three: Edited to specify a timeout period of at least 10 microseconds. Elimination of the 5 to 10 microsecond range is necessary for compatibility with early TURBOchannel option designs.
- *I/O Transactions*, paragraph four: Augmented to note that there may be other intervening I/O transactions before a conflicting I/O transaction is reissued. This may occur in systems that do not preserve ordering of processor read and write transactions. For example, if an I/O write from a write buffer is conflicting, then a higher priority I/O read, posted after the write, may be issued before the write is reissued. Analogous scenarios are possible with I/O writes issued before conflicting I/O reads are reissued.
- *I/O Addressing*, paragraph one: Last sentence corrected to indicate 27 address bits.
- *I/O Addressing*, paragraph four: Augmented to indicate that ordering of physical slots in the address space is system-specific, and that there may be address-space gaps between slots. This is necessary for implementations with TURBOchannel slots connected through intermediate adapter logic that may itself require some address space.
- *DMA read (1 word)* figure: Signal *~ack* cannot reassert until t6 to provide at least one deassertion cycle after data burst.
- *DMA*, paragraph seven: Augmented to indicate that systems with parity checking enabled assert *~err* if incorrect parity is detected on *ad*.
- *Parity*, paragraph two: Deleted to correct an editorial error.
- *Interrupts*: Section was added to clarify that interrupts are level-sensitive and that slot priority is system-specific.
- *Clock*, paragraph four: Added to indicate that clock phase and frequency variations may exist between different option slots. This may be the case for systems that connect TURBOchannel slots to an asynchronous memory subsystem through repeater logic, or to a memory subsystem through a crossbar interconnect.
- *Power*, paragraph four: Added metric specification of airflow. Also specified that airflow obstructions must be uniformly distributed to avoid creation of large airflow dead zones.
- *ROM*: ROM information reduced in this specification and referred to the *"TURBOchannel Firmware Specification."*

- *Mechanical Overview*, paragraph one: Augmented to indicate that physical slot numbering is system-specific.
- *Mechanical figure*: Added metric units and notation that units are in inches (centimeters). Changed airflow to indicate that it may be from either left-to-right or right-to-left. Changed bulkhead to reflect that dimensions are the maximum usable connector area.

Changes in Version 2A

- *DMA*, paragraph three: Augmented to indicate that deassertion of *~rReq* and *~wReq* may not occur until after *~ack* is asserted by the system.
- *Interrupts*: Added clarification of signal *~int* to indicate that once asserted, the option may not deassert *~int* until software dismisses the interrupt condition.
- *Implementation Notes*, paragraph one: Changed to clarify signal deassertion/assertion during reset and when the option is not selected.

Changes in Verison 2B

- *Table 3. Timing Requirements for TURBOchannel Signals*: Revised minimum times for *~rdy*, *~conflict*, *~int*, *~rReq*, *~wReq* to 1 nanosecond.
- *Implementation Notes*, paragraph eight: Added to clarify that an *~err* signal is valid for an option only when the option has asserted its *~ack* signal.

TURBOCHANNEL HARDWARE SPECIFICATION

General Description. The TURBOchannel is a synchronous, asymmetrical I/O channel. The beginning of a TURBOchannel cycle is defined by the rising edge of the channel clock signal (*clk*); all signals are specified with respect to that clock edge. A TURBOchannel can be operated at any fixed frequency in the range of 12.5 MHz to 25 MHz.

The TURBOchannel is asymmetrical: Connected to it is one *system* module and some number of *option* modules. Generally, the system module contains the main memory system and the processor, and the option modules contain controllers for peripheral devices.

Two kinds of transactions are permitted on the TURBOchannel: The system module can read or write an option module (an *I/O transaction*), and an option module can read or write the system module (a *DMA transaction*). An option module cannot address another option module on the TURBOchannel.

Systems can time-multiplex multiple option slots onto a single memory port to share its bandwidth, or systems can dedicate a memory port to each option slot.

Signals. Table 1 lists the source and function of each signal on the TURBOchannel. Signals prefaced by a tilde (~) are active-low. Signals without a tilde are active-high.

Table 1. TURBOchannel Signals

Signal Name	Source	Function
ad[P, 31..0]	bussed	Address/data bus
~sel	system	I/O read/write select
~write	system	I/O read/write specifier
~ack	system	DMA read/write acknowledge
~err	system	DMA error
~reset	system	System reset
clk	system	Channel clock
~rdy	option	I/O read/write ready
~conflict	option	I/O read/write conflict
~rReq	option	DMA read request
~wReq	option	DMA write request
~int	option	I/O interrupt

The meaning of the *ad* lines depends on the type of transaction and whether it is an address or data phase of that transaction type.

Transactions. The minimum length of a TURBOchannel transaction is two clock cycles. Some system implementations may be able to achieve back-to-back transactions; others may insert idle cycles in between. The only exception is that back-to-back I/O transactions to the same option must have an idle cycle in between, guaranteeing the deassertion of select to that option.

Idle Cycles. During idle channel cycles, the system drives the *ad* lines.

I/O Transactions. Processor load/store instructions to the I/O slot address range generate I/O read/write transactions. As the system drives the address onto the TURBOchannel, it decodes the address and asserts a select signal (~*sel*) for the specified option slot.

For read transactions, the system waits for the slot to drive data onto the TURBOchannel and assert its ready signal (~*rdy*). For write transactions, the system drives data onto the TURBOchannel until the option asserts its ready signal. Figure 1 shows signal activity when a system performs an I/O read of an option. Figure 2 shows signal activity when a system performs an I/O write to an option.

Options should minimize ready assertion latency to maximize channel utilization. If the option does not respond within the system-specified timeout period, the system aborts the transaction. The timeout period for a particular system is listed in the system guide and must be at least 10 microseconds.

The ~*conflict* signal can be used by an option to tell the system that the option is already committed to a DMA transaction and cannot respond to an I/O transaction. The ~*conflict* signal should be asserted with ~*rdy* and only when the option is selected. Because this mechanism adversely affects system performance and interrupt service latency, ~*conflict* should be used only when it is the only means of breaking a deadlock. The system *may* retry the I/O transaction at some future time. There may be other intervening I/O transactions before a conflicting I/O transaction is reissued.

I/O Addressing. Each slot has a 4- to 512-Mbyte address range for I/O transactions. The size of the slot address space is system-specific in power-of-two multiples. For systems with less than 512-Mbyte spaces, the high-order address bits are undefined and must be treated as *don't care* values. Options should decode internal logic on the minimal number of low order address bits. Addresses are 27-bit word addresses; therefore, the least significant two address bits of the byte address are implicitly zero.

Figure 3 shows the interpretation of the *ad* signals during an I/O read address cycle. Bits *ad*[31..5] specify the word address within the slot space. The option responds by driving the addressed word onto *ad*.

Figure 4 shows the interpretation of the *ad* signals during an I/O write address cycle. Bits *ad*[31..5] specify the word address within the slot space. Bits *ad*[4..1] specify byte masks for the *ad* signals during the subsequent data cycle of the transaction. If a byte mask bit is one, the corresponding byte lane is not stored in the addressed word.

The number of slots, size of the slot space, and base address of the slots are system-specific. Ordering of physical option slots in the address space is also system specific. There may by system-specific gaps in the address space between adjacent physical option slots. The address space must be documented in the system guide.

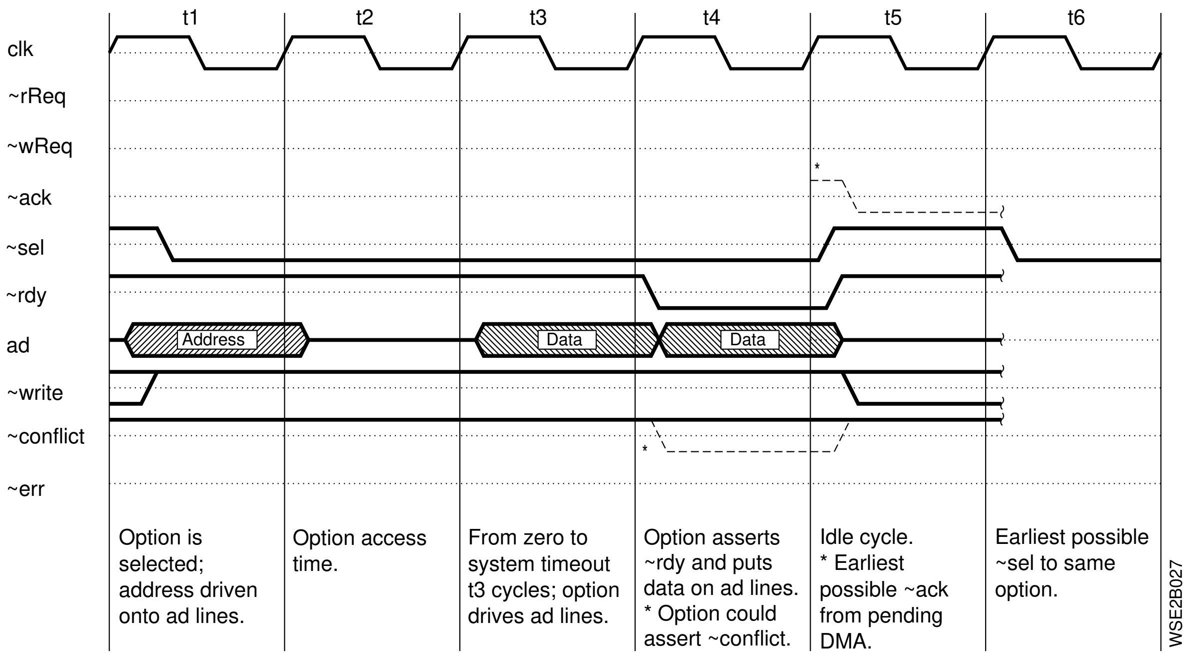

Figure 1. I/O read of an option by the system

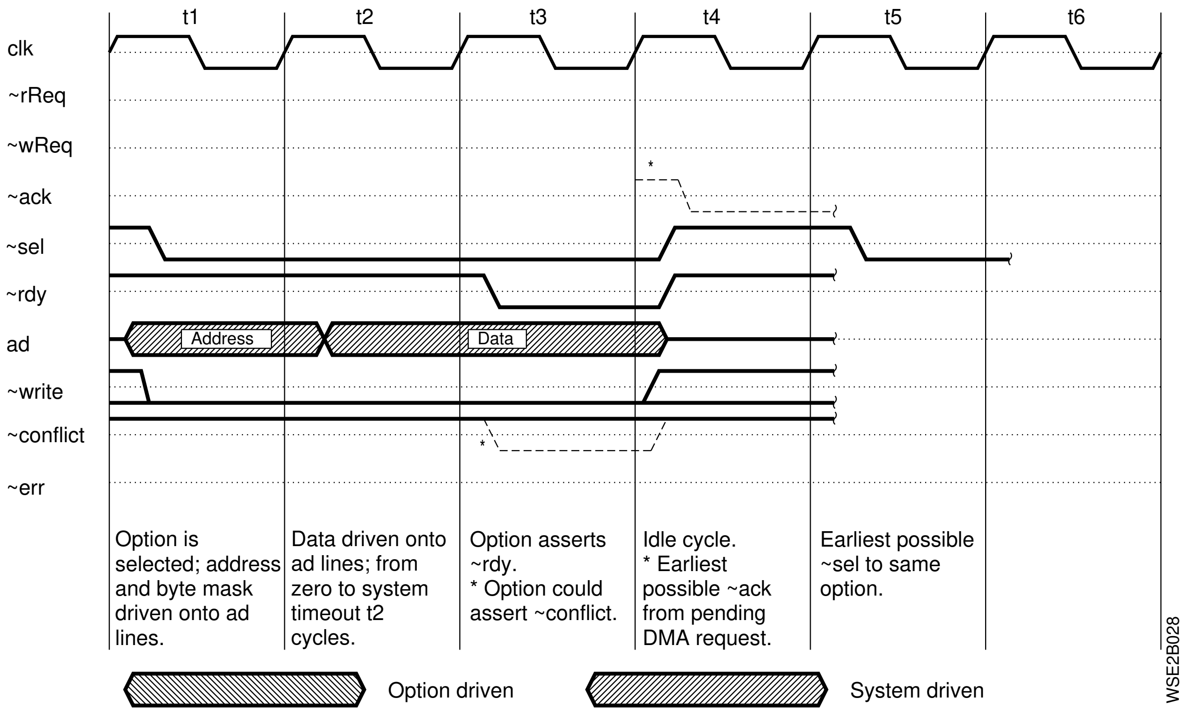

Figure 2. I/O write to an option by the system

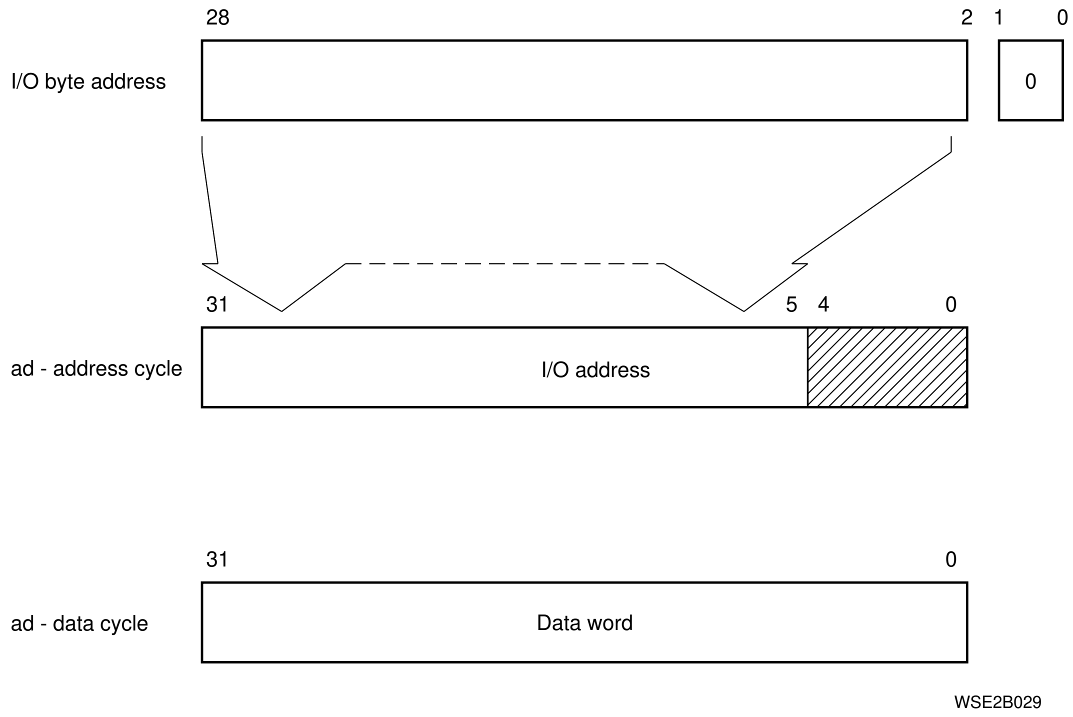

Figure 3. Interpretation of the *ad* signal during an I/O read

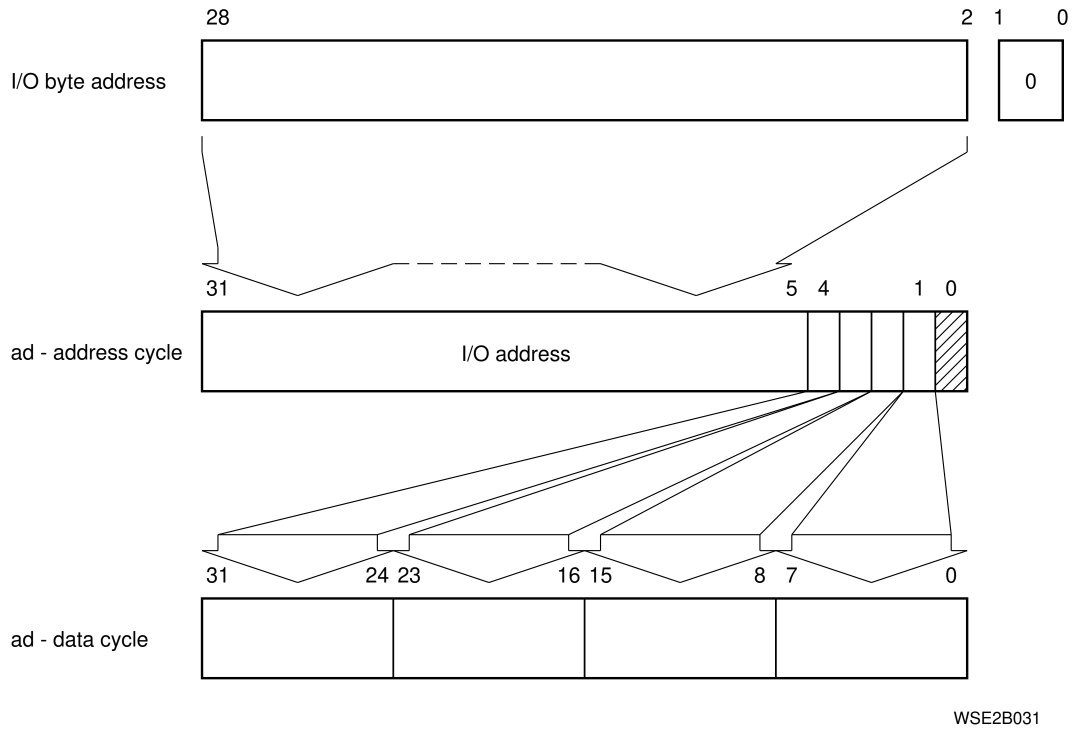

Figure 4. Interpretation of the *ad* signal during an I/O write

DMA. TURBOchannel DMA transactions are always in units of 32-bit words and can be of any length up to an implementation-defined limit. That limit is guaranteed to be at least 64 words and to be a power-of-two. To obtain the best possible performance, the data words are transmitted one per cycle. Once the first DMA read data word is available, subsequent data words of the block are available (and must be accepted) in every cycle. DMA write data words are accepted (and must be supplied) in every cycle.

The arbitration of requests for DMA transactions is implementation-specific. Although fixed-priority schemes are encouraged for some specified slot to achieve full bandwidth, other schemes, such as fair service, are legal. The guide for a particular system must describe the arbitration scheme used.

An option requests a DMA transaction by asserting either signal *~rReq* or signal *~wReq* and must not assert both signals simultaneously. Once asserted, the option may not deassert signal *~rReq* or *~wReq* until the system grants service by asserting signal *~ack*. The option indicates the block length by the number of cycles that it continues to assert signals *~rReq* or *~wReq* after signal *~ack* is asserted by the system.

Addresses for DMA transactions define a 16-Gbyte address space (34 address bits). The upper five address bits are presented in *ad*[4..0]. Bits *ad*[31..5] form the rest of the word address; the low-order two address bits are implicitly zero. Figure 5 shows the interpretation of a DMA transaction *ad* signal.

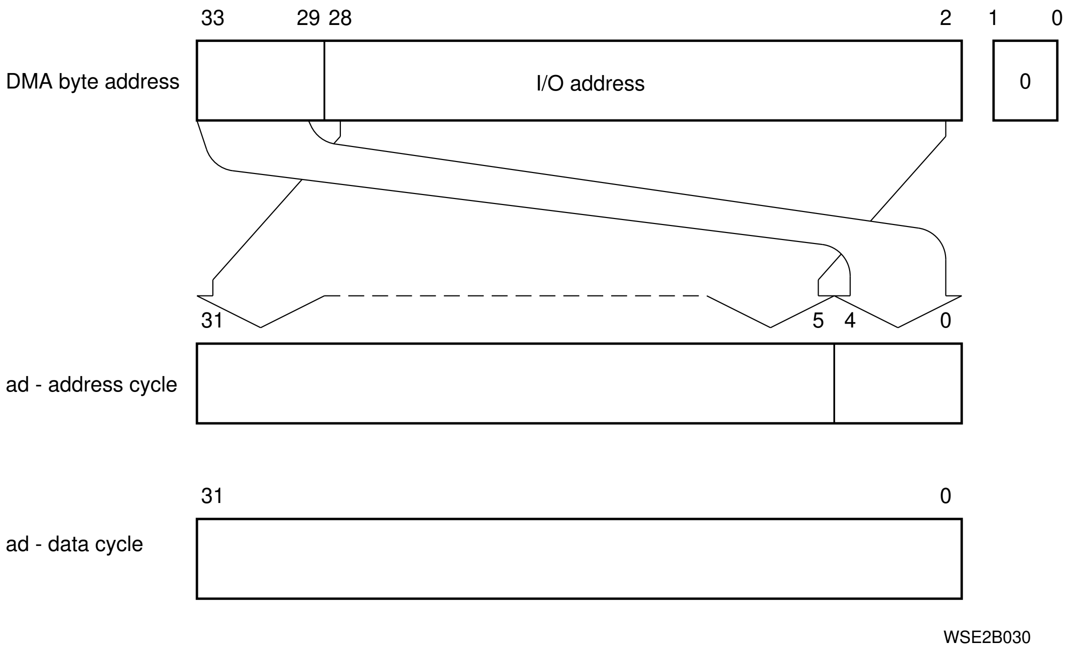

Figure 5. Interpretation of the *ad* signal during a DMA transaction

A given system may not support the entire address space; the consequences of addressing nonexistent memory in a DMA transaction is implementation-dependent.

The high performance of the TURBOchannel, in which a word is transmitted in every channel cycle, may require some implementations to use page-mode accesses to the system memory dynamic RAMs. DMA transactions cannot cross 2048-byte address boundaries.

If an uncorrectable memory error occurs during a DMA read transaction, the system asserts signal *~err* along with the uncorrectable data. If an option requests more than the maximum block size for a DMA read or write transaction, the system asserts signal *~err*. If parity checking is enabled and the system detects incorrect parity on the *ad* signals, the system asserts signal *~err*. The option must terminate its DMA transaction on the cycle immediately after the *~err* signal is asserted.

In the case of DMA read errors, the *~ack* signal can remain asserted for several cycles (if the memory is pipelined, for example). Option logic must be designed to avoid misinterpreting an *~ack* signal from an aborted transfer as the *~ack* signal for a subsequent DMA request.

Figures 6 and 7 show signal activity when an option performs a one-word or two-word DMA read of the system. Figures 8 and 9 show signal activity when an option performs a one-word or two-word DMA write to the system.

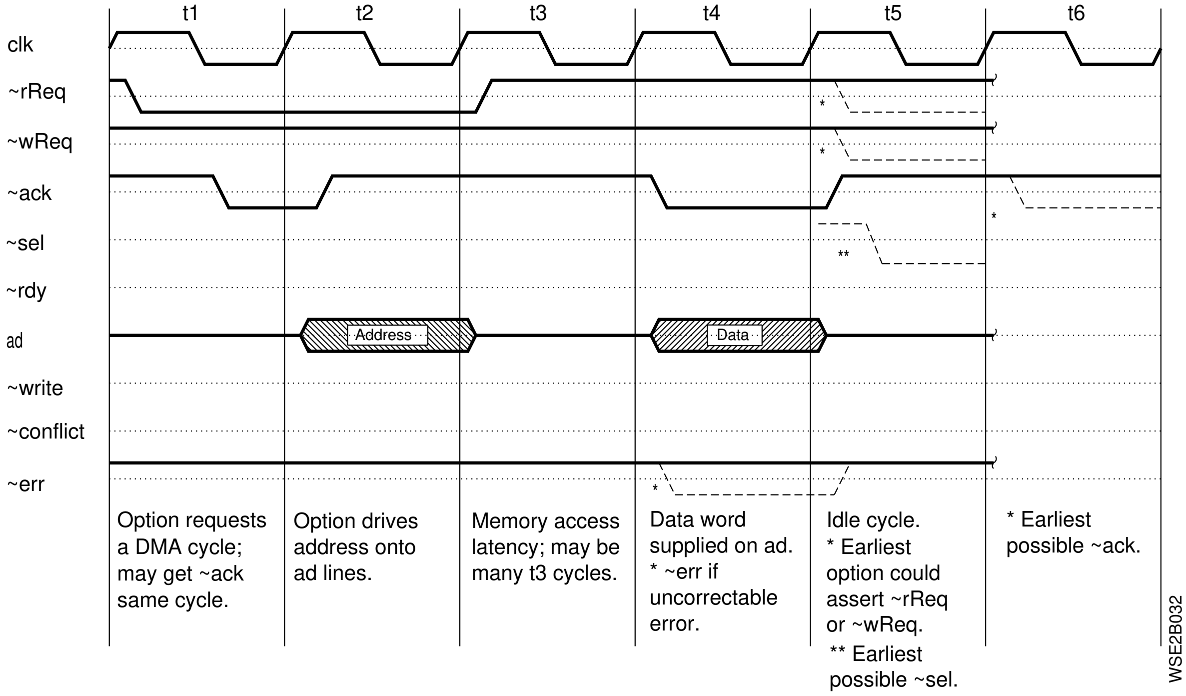

Figure 6. One-word DMA read of the system by an option

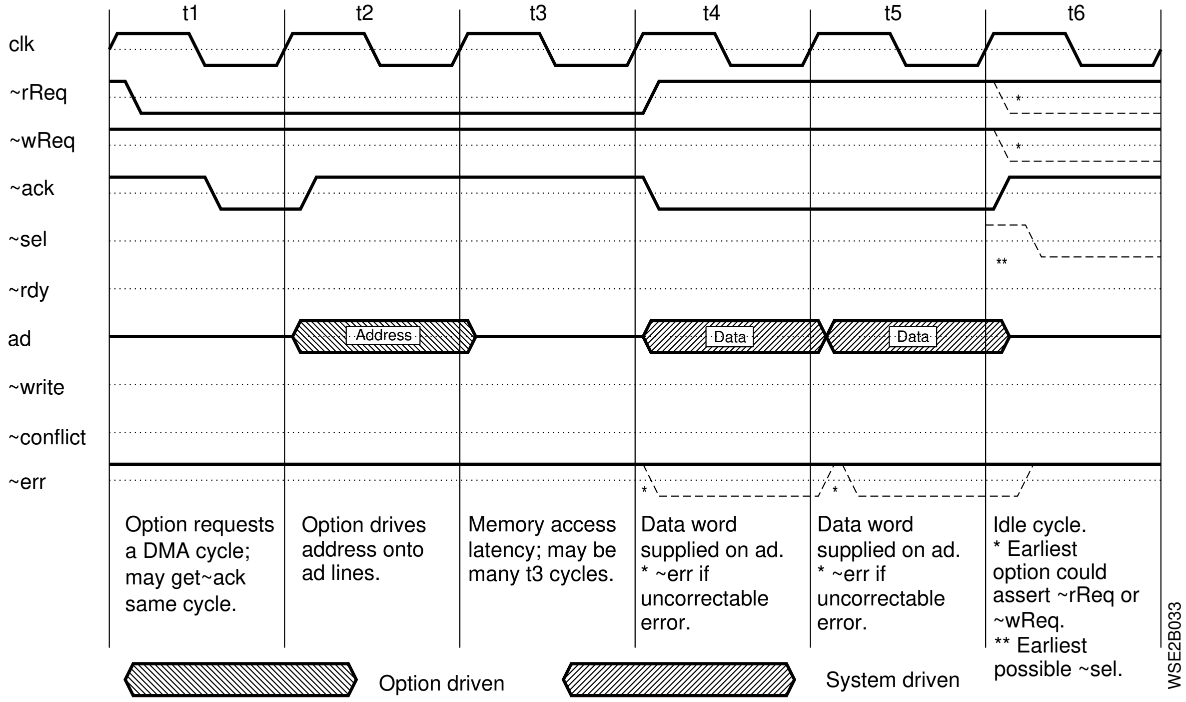

Figure 7. Two-word DMA read of the system by an option

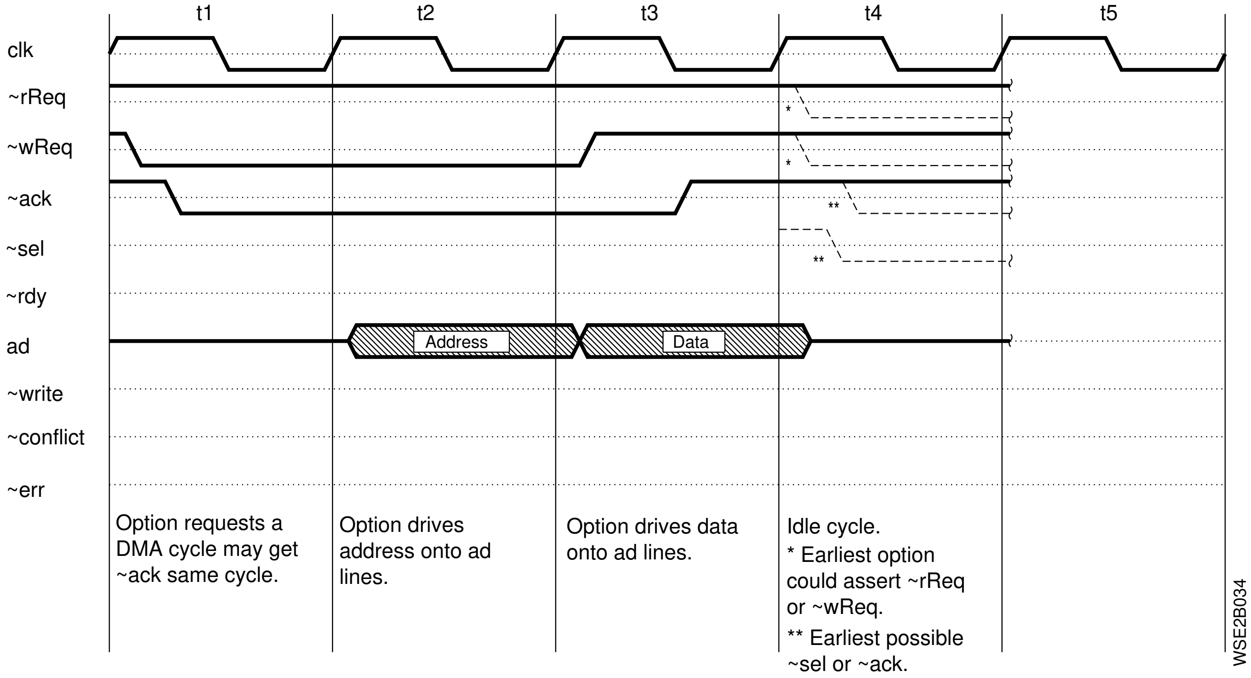

Figure 8. One-word DMA write to the system by an option

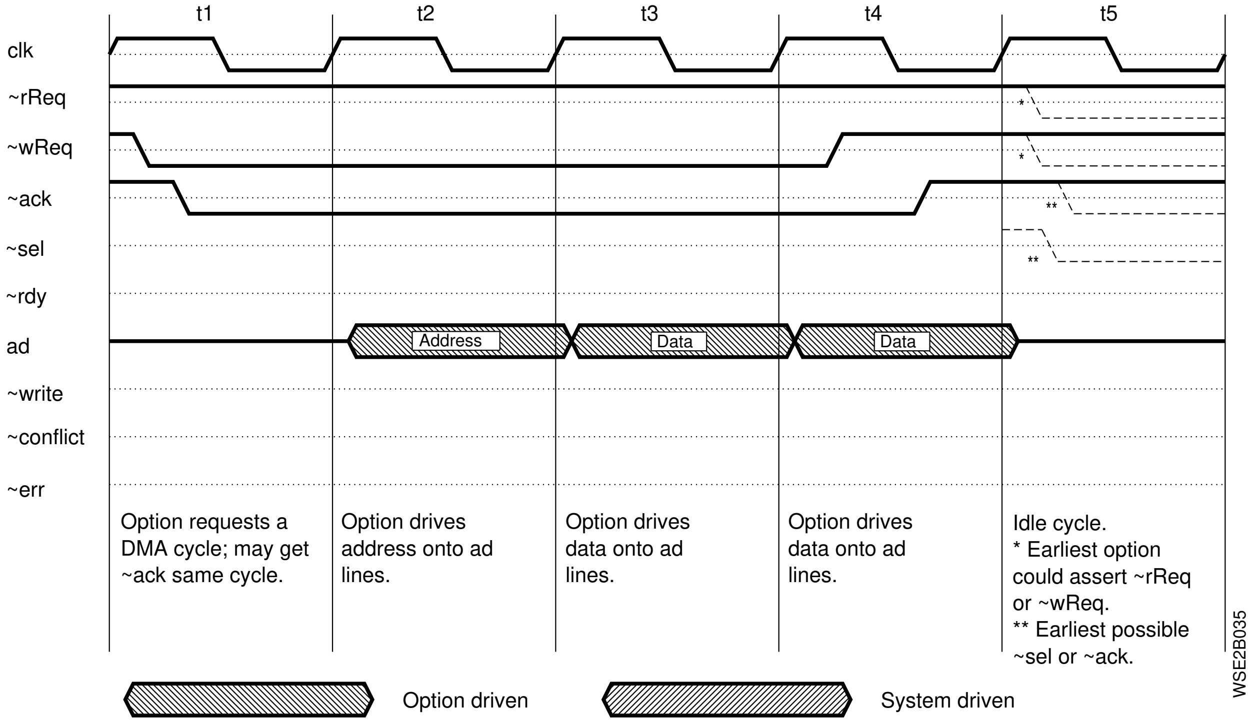

Figure 9. Two-word DMA write to the system by an option

Parity. Options may implement odd word parity for the *ad* signals on the *ad[P]* signal. Options that implement parity must provide a means for enabling and disabling parity checking under software control. Parity checking must be disabled by the assertion of the *~reset* signal. When parity checking is enabled, the option must check parity when it accepts an I/O read address, an I/O write address, I/O write data, or DMA read data. If the option detects a parity error, it should record this event in some fashion and initiate appropriate higher level error notification. System implementations that support parity should be designed to simultaneously handle mixtures of options, some of which have parity enabled, and some of which do not implement parity.

Interrupts. Interrupts are level-sensitive with slot priority determined by system hardware and software. Once asserted, the option may not deassert signal *~int* until software dismisses the interrupt condition.

Electrical. For bussed signals (*ad*[P, 31..0]) on a TURBOchannel, the system module plus options must present no more than 180 pF capacitive load. The total trace length for any bussed signal cannot exceed 16 inches on the system module. An option module must present no more than 20 pF capacitive load to any bussed signal. The total trace length on an option module for a bussed signal cannot exceed 2 inches. Capacitance measurements must include all connectors, components, lands, and traces.

For system-generated control signals, the load imposed by an option module cannot exceed 50 pF including the connector, all components, lands, and traces, except for the clock signal which is 100 pF.

For option-generated control signals, the load imposed by the system module cannot exceed 65 pF including the connector, all components, lands, and traces.

A multi-slot-width option must only connect signals to one slot, though it can draw power from all connectors.

Table 2 lists the DC parameters for TURBOchannel signals.

Table 2. DC Parameters for TURBOchannel Signals

Value	*ad*[P, 31..0]	System-generated	Option-generated
Voh	2.4 V (min)	same	same
Vih	2.0 V (max)	same	same
Vil	0.8 V (min)	same	same
Vol	0.5 V (max)	same	same
Iih	+70 uA(max)	+0.5 mA(max)	+0.5 mA(max)
Iil	-70 uA(max)	-1.5 mA(max)	-1.5 mA(max)
Ioh	-1.0 mA(min)	same	same
Iol	+2.0 mA(min)	same	same

Timing. Table 3 lists the propagation delay from the rising edge of the *clk* signal for each of the TURBOchannel signals. All times are in nanoseconds. The setup and hold times specified for system-generated signals must be met at each option in the system and are measured with respect to the clock at that option. The delays for option-generated signals are measured on the option with respect to the clock at the option and with the full capacitive loading on all signals from the option.

Table 3. Timing Requirements for TURBOchannel Signals

Signal	Source	Min	Max	Setup	Hold
ad	system			5	2
ad to 3-state	system	3	22		
~sel, ~write, ~ack, ~err, ~reset	system			13	2
ad	option	3	34		
ad to 3-state	option	3	22		
~rdy, ~conflict, ~int	option	1	12		
~rReq and ~wReq	option	1	7		

Clock. The TURBOchannel uses a free-running clock (*clk*) that can be at any fixed frequency in the range 12.5 MHz through 25 MHz. The rise and fall times of the clock signal must not exceed 5 ns as measured at the *clk* signal pin on the connector of an option. The clock signal must be high for at least 15 ns and low for at least 15 ns.

Figure 10 shows the timing requirements for each phase of the *clk* signal.

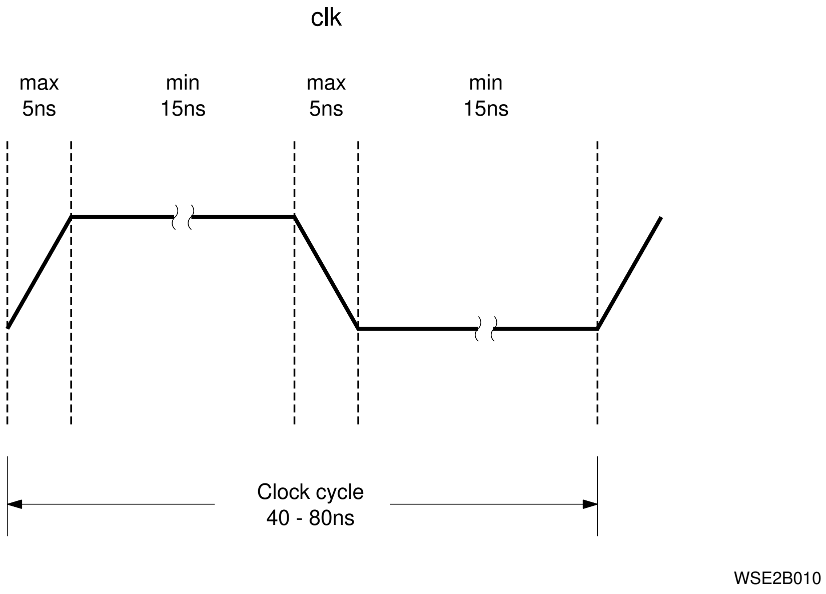

Figure 10. Timing requirements for the *clk* signal

Clock skew between the system module and the option modules must be controlled so that the system module functions correctly for any modules meeting the delay specifications listed above.

Systems can have clock phase and frequency variations between different physical option slots.

An option module must have a diode terminator to ground and a diode terminator to the +5 Volt supply for its *clk* signal.

Power. A TURBOchannel system module provides two supply voltages to each TURBOchannel option: +5 V and +12 V. The sequencing of the +5 V and the +12 V supplies is not guaranteed.

Table 4 describes the voltage and current a that are available to a TURBOchannel option.

Table 4. Power Available to TURBOchannel Options

	Maximum Current		
Voltage	**Single-Width Option**	**Double-Width Option**	**Triple-Width Option**
+5 V ±5%	4.0 A	8.0 A	12.0 A
+12 V ±5%	0.5 A	1.0 A	1.5 A

The signal *~reset* is asserted for at least 250 milliseconds after power is switched on and the +5 V supply has become stable. The *~reset* signal is reasserted at least 500 microseconds before the +5 V supply drops.

The system will maintain an airflow of at least 50 linear feet-per-minute (LFM) (25 centimeters-per-second (CM/S)) below an option module. The system will maintain an airflow of at least 150 LFM (76 CM/S) above an option module. An option module must not obstruct more than 50% of the side-to-side cross-sectional area above itself with components or daughter cards. Module obstructions must be uniformly distributed so there are no downstream airflow *dead zones*.

Implementation Notes. During reset, an option must deassert the *~rdy*, *~conflict*, *~rReq*, *~wReq*, and *~int* signals and three-state the *ad* signals. An option must not assert *~rdy* or *~conflict* signals when it is not selected. Thus, a system need not qualify these signals with the option select line.

Options that do not implement the following features should not connect to the corresponding signals:

parity	*ad*[P]
I/O conflicts	*~conflict*
DMA	*~wReq*, *~rReq*, *~ack*, or *~err*
interrupts	*~int*

Options that do not have 32-bit internal data paths must still drive all 32 *ad* signals when supplying I/O read data.

Options that cannot address the entire 16-Gbyte DMA address space must drive zero onto high-order address signals.

Designers must use good engineering practices in selecting logic families to implement the system and option interfaces. This implies the use of the slowest logic that meets the timing requirements of the TURBOchannel, and internal clamping to control signal reflections.

Designers must use good engineering practices in decoupling the supply voltages on system and option modules.

Options should meet all specifications while operating in office environments of 10° C to 40° C ambient temperature plus 10° C internal rise and 10% to 90% relative humidity. Options should be designed to meet appropriate international class A electromagnetic interference regulations and international safety regulations. Options should be designed with appropriate electrostatic discharge protection for their application as well as routine shipping and installation handling.

Systems that time-multiplex option slots onto a single memory port may distribute common *~write* and *~err* signals to multiple slots. Options may observe transitions of these signals during transactions to other option slots. The *~write* signal is only valid for an option when its *~sel* signal is asserted. The *~err* signal is only valid for an option when its *~ack* signal is asserted.

Connector. The TURBOchannel uses a 96-pin DIN connector. Female connectors are used on the system module and male connectors on the option modules. Suggested connectors are the AMP 532504-1 (female) and the AMP 532523-1 (male). Options must not connect to the four NC pins. Table 5 lists the pin assignments for a TURBOchannel connector.

Table 5. TURBOchannel Connector Pin Assignments

Row	Column A	Column B	Column C
1	*ad*[31]	GND	*ad*[30]
2	*ad*[29]	GND	*ad*[28]
3	*ad*[27]	GND	*ad*[26]
4	*ad*[25]	GND	*ad*[24]
5	+5 V	GND	+5 V
6	*ad*[23]	GND	*ad*[22]
7	*ad*[21]	GND	*ad*[20]
8	*ad*[19]	GND	*ad*[18]
9	*ad*[17]	GND	*ad*[16]
10	+5 V	GND	+5 V
11	*ad*[15]	GND	*ad*[14]
12	*ad*[13]	GND	*ad*[12]
13	*ad*[11]	GND	*ad*[10]
14	*ad*[9]	GND	*ad*[8]
15	+5 V	GND	+5 V
16	*ad*[7]	GND	*ad*[6]
17	*ad*[5]	GND	*ad*[4]
18	*ad*[3]	GND	*ad*[2]
19	*ad*[1]	GND	*ad*[0]
20	+5 V	GND	+5 V
21	NC	GND	NC
22	NC	GND	NC
23	*~conflict*	GND	*ad*[P]
24	*~ack*	GND	*~err*
25	+5 V	GND	+12 V
26	*~rReq*	GND	*~wReq*
27	†	GND	*~write*
28	*~sel*	GND	*~rdy*
29	*~int*	GND	*~reset*
30	GND	GND	GND
31	GND	*clk*	GND
32	GND	GND	GND

†Called *~iaCE* in prototype implementations. It is similar to *~sel* but is asserted only for the first cycle of the I/O transaction. Option modules should not use this signal.

ROM. Every TURBOchannel option module must have a ROM as defined by the *"TURBOchannel Firmware Specification"*. The ROM must contain certain information about itself and the identity of the option. The ROM may also contain additional option firmware.

Mechanical Overview. Figure 11 illustrates the space available to an option module inside a DECstation/DECsystem 5000 Model 200 system unit. For detailed mechanical control drawings refer to EK-TCAAC-OM-003. Physical option slot numbering is system-specific and must be documented in the system guide.

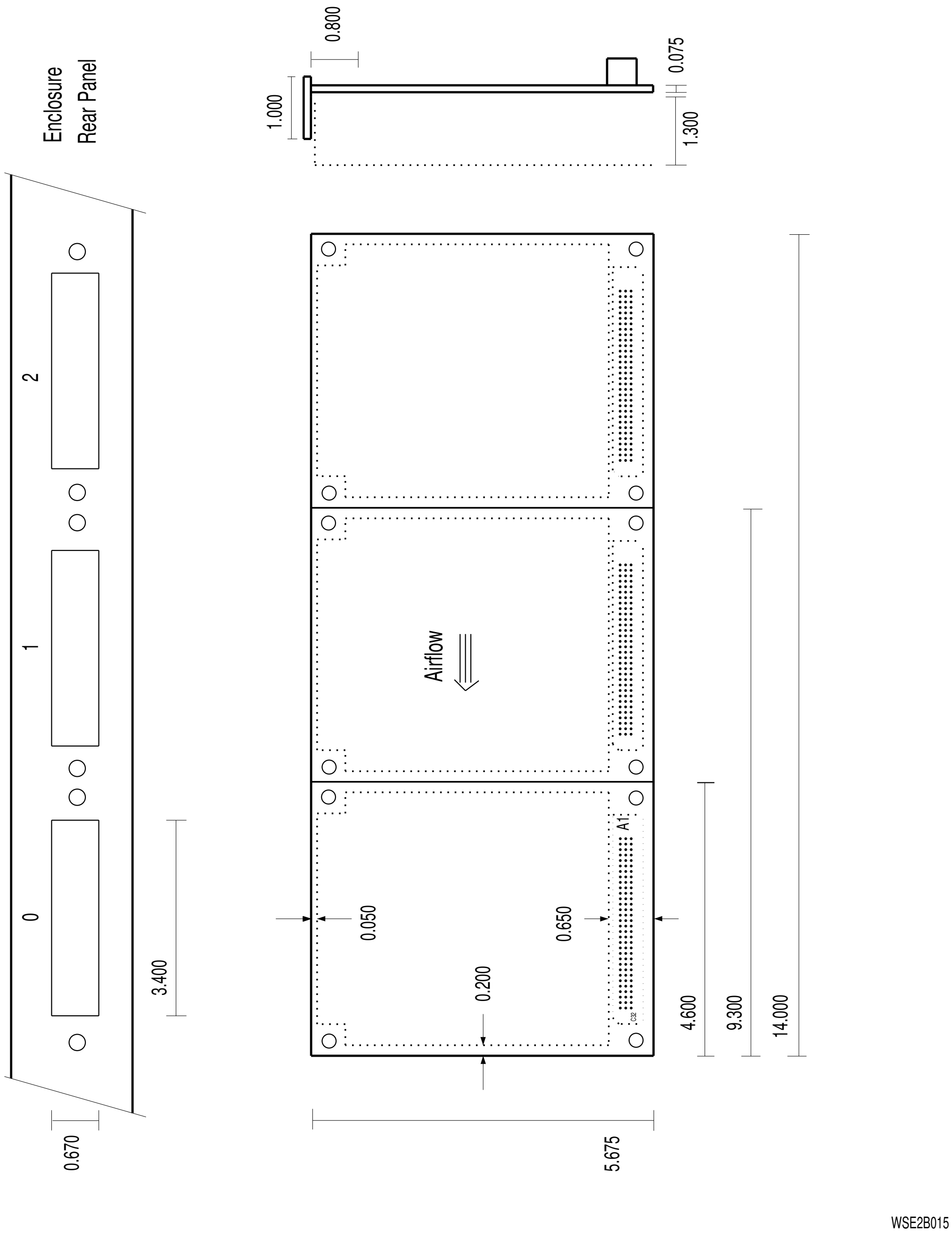

Figure 11. Space available for TURBOchannel modules inside a DECstation/DECsystem 5000 Model 200